THIS IS AN IMPEDANCE CONTROLLED BOARD.

NOTE :
1. ALL CORE AND PREPREG THICKNESSES ARE UP TO FAB SHOP TO SELECT.
2. EXTERNAL LAYER CU THICKNESSES ARE FINISHED THICKNESS AFTER PLATING.

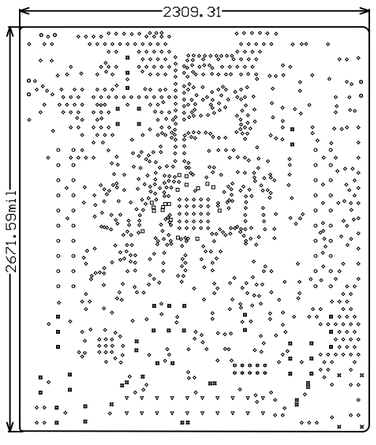
## IMPEDANCE TABLE

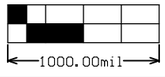
| LAYER NO | CONDUCTOR WIDTH | SPACING | IMPEDANCE +/- 10% | REFERENCE GND |
|---|---|---|---|---|
| 1 | 10.25 | 15.5 mil | 50 OHMS | GND |

| Symbol | Quantity | Finished Hole Size | Plated | Hole Type | Drill Layer Pair | Hole Tolerance |
|---|---|---|---|---|---|---|
| ✪ | 6 | 35.43mil (0.900mm) | NPTH | Round | Top Layer - Bottom Layer | |
| ◇ | 854 | 7.87mil (0.200mm) | PTH | Round | Top Layer - Bottom Layer | |
| □ | 19 | 8.00mil (0.203mm) | PTH | Round | Top Layer - Bottom Layer | |
| ⊠ | 14 | 12.00mil (0.305mm) | PTH | Round | Top Layer - Bottom Layer | +0.00mil/-4.00mil |
| ✡ | 10 | 27.95mil (0.710mm) | PTH | Round | Top Layer - Bottom Layer | |
| ▽ | 20 | 40.16mil (1.020mm) | PTH | Round | Top Layer - Bottom Layer | +/-7.87mil |
| ○ | 40 | 40.16mil (1.020mm) | PTH | Round | Top Layer - Bottom Layer | |
| ◙ | 39 | 45.28mil (1.150mm) | PTH | Round | Top Layer - Bottom Layer | |
| ⌑ | 4 | 47.24mil (1.200mm) | PTH | Slot | Top Layer - Bottom Layer | |
| | 1006 Total | | | | | |

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

| Layer | Name | Material | Thickness | Constant | Board Layer Stack |
|---|---|---|---|---|---|
| | Top Overlay | | | | |
| | Top Solder | Solder Resist | 1.00mil | 3.5 | |
| 1 | Top Layer | | 1.85mil | | |
| | Dielectric 1 | FR-4 High Tg | 5.48mil | 4.2 | |
| 2 | LO2_GND | | 1.26mil | | |
| | Dielectric1 | FR-4 High Tg | 42.82mil | 4.2 | |
| 3 | LO3_PWR | | 1.26mil | | |
| | Dielectric 2 | FR-4 High Tg | 5.48mil | 4.2 | |
| 4 | Bottom Layer | | 1.85mil | | |
| | Bottom Solder | Solder Resist | 1.00mil | 3.5 | |
| | Bottom Overlay | | | | |




| DESIGN INFORMATION | |
|---|---|
| MIN. TRACK WIDTH: | 5 MIL |
| MIN. CLEARANCE: | 4 MIL |
| MIN. VIA PAD SIZE: | 14 MIL |

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-4 ☒ FR-4 High Tg ☐ OTHER _____
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER _____
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER _____

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER _____
SOLDER RESIST COLOR: ☐ GREEN ☒ OTHER RED
☒ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER _____

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☒ N.C. ROUTE ☐ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☒ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: LP-EM-CC35X1
DESIGNED FOR: Public Release
FILE NAME: MCU138A_LP-EM-CC35X1.PcbDoc

| ALL ARTWORK VIEWED FROM TOP SIDE | BOARD #: MCU-138 | REV: A | SVN REV: dcf40d21423adf2ac2a963694f23e8051f936a43 (Locally Modified) |
|---|---|---|---|
| LAYER NAME = [illegible] | TID #: N/A | | |
| PLOT NAME = Fabrication Drawing | GENERATED : 12/24/2025 5:40:25 PM | TEXAS INSTRUMENTS | |

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| ENGINEER: | LAYOUT BY: |
|---|---|
| Jonathan Cohen | Jonathan Cohen |
| SCALE: 1.00 | ALTIUM DESIGNER VERSION: 23.1.1.15 |